UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,604	08/22/2003	David Feldmeier	M4065.0573/P573-B	8591

			EXAMINER
24998	7590	08/17/2004	ANDERSON, MATTHEW D

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

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DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 August 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>56-87</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>56-87</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>22 August 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/10/04</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   In response to the amendment filed 8/22/03:

claims 1-55 have been canceled;

the specification has been amended.

Double Patenting

2.   The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA

1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this

application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

2.   Claims 62-64, 71-72, and 78-81 are rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 31-32 of U.S. Patent No.

6,289,414. Although the conflicting claims are not identical, they are not patentably distinct

from each other because of the following:

3.   Claims 62-63 and 71 of the present application teach similarly with claim 31 of US Patent #

6,289,414.

4.   Claims 64 and 72 of the present application teach similarly with claim 32 of US Patent #

6,289,414.

5.   Broad claim 78 of the present application is taught by the more specific claim 1 of US Patent

6,289,414.

6.   Broad claims 79-81 of the present application is taught by the more specific claims 19, 22,

and 31 of US Patent # 6,289,414.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4.   Claims 56-87 are rejected under 35 U.S.C. 102(a) as being anticipated by Music

Semiconductor Application Note AN-N22 (*A Method* For Fast IPv4 And IPv4 CIDR Address*

Translation And Filtering Using The MUSIC WidePort LANCAM ®, LANCAM ® , AND

LANCAM ® 1 ST Family), hereinafter "LANCAM".

5.   With respect to claims 56, 62, 65, 71, 73, and 77-81, LANCAM discloses:

a binary CAM for storing ternary hierarchical addresses comprising a communication

system address and associated communication system address mask, as shown in Table 5;

each entry comprising a first value comprising the logically ANDed communication

system address and its associated mask (as described on page 4), and a second value comprising

the logically ANDed complement of said communication system address and its associated mask

(as described on page 4), wherein each entry is positioned in the CAM based on the number of

contiguous ones in said associated mask as described on page 2;

each entry comprising a two bit representation for each bit in said address, as disclosed in

pages 2-3;

storing ternary entries in a binary CAM, as disclosed in pages 6-8;

6.   With respect to claims 57, 64, 66, and 72, LANCAM discloses entries having the most

contiguous ones located at the top of the CAM, and the least contiguous ones at the bottom of the

CAM, as described in page 2.

7.   With respect to claims 58 and 67, LANCAM discloses each of said n bits in said first

value has an associated bit in said second value, and each of the bits and associated bit forming a

binary pair which represents one bit of said address as two bits in the CAM, as described in page

4.

8.   With respect to claims 59, 63, 68, and 71, LANCAM discloses a 1 in the address

representing a 10 in the CAM, a 0 in the address representing a 01 in the CAM, a don't care in

the address representing a 00 in the CAM, as disclosed in page 3.

9.   With respect to claims 60-61, 69-70, and 75-76, LANCAM discloses the first value being

stored in an upper portion of said entry and the second value in a lower portion, with each entry

being 64 bits and n being 32, as shown in Table 5.

10.   With respect to claims 73 and 77, LANCAM discloses searching a binary CAM to find a

match of a ternary address by loading a first register with the address to be searched along with

the complement of the address, loading the second register with the address to be searched along

with the complement of the address, and associating each bit of the first register with one bit of

the second register and with one bit of each entry in said binary CAM, determining whether a bit

match occurs, and obtaining a match based on the greatest number of matches of corresponding

bits, as disclosed on page 8 and in Table 7.

11.   With respect to claims 74 and 77, LANCAM discloses declaring a bit match if the

corresponding bit in the second register is a 1, or if the corresponding bit in the second register is

a 0 and the corresponding bits of the first register and each entry in the binary CAM are

identical, as disclosed in page 8 and Table 7.

12.   With respect to claims 78-81, LANCAM discloses:

        segmenting the binary CAM into blocks and arranged in the CAM such that the lowest

CAM addresses contain the highest masks, and the highest Cam address contain the lowest

masks, as disclosed in page 2;

        storing addresses according to said block having a corresponding mask, as shown in page

2;

        tracking the first address and the next free address of each of said blocks and the size of

each block, as shown in page 5.

binary-encoding ternary conversion means wherein a 1 in the address representing a 10 in

the CAM, a 0 in the address representing a 01 in the CAM, a don't care in the address

representing a 00 in the CAM, as disclosed in page 3.

13.   With respect to claim 82, LANCAM discloses a first group of address entries sharing a

first said address mask and a second group of address entries sharing a second said address mask,

said first and second groups being located at different locations of the CAM, as taught on page 3.

14.   With respect to claim 83, LANCAM discloses comprising at least one vacant

address entry location disposed within said CAM between said first and second groups of

address entries, as shown in figures 5, 6, and 8.

15.   With respect to claim 84, LANCAM discloses at least one vacant address entry location

within said CAM adjacent at least one of said address entry groups, as shown in figures 5, 6, and

8.

16.   With respect to claim 85, LANCAM discloses: receiving an address value in a

comparand register of said CAM; matching a further plurality of addresses, including a subset of

said communication system hierarchical addresses, to said address value; and outputting an

output hierarchical address of ,said further plurality of addresses according to respective storage

locations of said further plurality of addresses, as shown in Table 7 on page 5.

17.   With respect to claim 86, LANCAM discloses wherein said output hierarchical address of

said further plurality has a storage location lowest among said respective storage locations of

said further plurality of addresses, as shown in Figure 3 on page 7.

18.   With respect to claim 87, LANCAM discloses wherein said further plurality of said

communication system hierarchical addresses each includes at least one identical bit, as shown in

Table 7 on page 5.

19.   Claims 56-87 are rejected under 35 U.S.C. 102(a) as being anticipated by Music

Semiconductor Application Note AN-N25 (*Fast IPv4 and IPv4 CIDR Address Translation and*

Filtering Using the MUACTM Routing Coprocessor (RCP)), hereinafter "RCP".

20.   With respect to claims 56, 62, 65, 71, 73, and 77-81, RCP discloses:

       a binary CAM for storing ternary hierarchical addresses comprising a communication

system address and associated communication system address mask, as shown in Table 5;

       each entry comprising a first value comprising the logically ANDed communication

system address and its associated mask (as described on page 4), and a second value comprising

the logically ANDed complement of said communication system address and its associated mask

(as described on page 4), wherein each entry is positioned in the CAM based on the number of

contiguous ones in said associated mask as described on page 2;

       each entry comprising a two bit representation for each bit in said address, as disclosed in

pages 2-3;

       storing ternary entries in a binary CAM, as disclosed in pages 6-8;

21.   With respect to claims 57, 64, 66, and 72, RCP discloses entries having the most

contiguous ones located at the top of the CAM, and the least contiguous ones at the bottom of the

CAM, as described in page 2.

22.   With respect to claims 58 and 67, RCP discloses each of said n bits in said first value has

an associated bit in said second value, and each of the bits and associated bit forming a binary

pair which represents one bit of said address as two bits in the CAM, as described in page 4.

23.   With respect to claims 59, 63, 68, and 71, RCP discloses a 1 in the address representing a

10 in the CAM, a 0 in the address representing a 01 in the CAM, a don't care in the address

representing a 00 in the CAM, as disclosed in page 3.

24.   With respect to claims 60-61, 69-70, and 75-76, RCP discloses the first value being

stored in an upper portion of said entry and the second value in a lower portion, with each entry

being 64 bits and n being 32, as shown in Table 5.

25.   With respect to claims 73 and 77, RCP discloses searching a binary CAM to find a match

of a ternary address by loading a first register with the address to be searched along with the

complement of the address, loading the second register with the address to be searched along

with the complement of the address, and associating each bit of the first register with one bit of

the second register and with one bit of each entry in said binary CAM, determining whether a bit

match occurs, and obtaining a match based on the greatest number of matches of corresponding

bits, as disclosed on page 8 and in Table 7.

26.   With respect to claims 74 and 77, RCP discloses declaring a bit match if the

corresponding bit in the second register is a 1, or if the corresponding bit in the second register is

a 0 and the corresponding bits of the first register and each entry in the binary CAM are

identical, as disclosed in page 8 and Table 7.

27.   With respect to claims 78-81, RCP discloses:

segmenting the binary CAM into blocks and arranged in the CAM such that the lowest

CAM addresses contain the highest masks, and the highest Cam address contain the lowest

masks, as disclosed in page 2;

storing addresses according to said block having a corresponding mask, as shown in page

2;

tracking the first address and the next free address of each of said blocks and the size of

each block, as shown in page 5.

binary-encoding ternary conversion means wherein a 1 in the address representing a 10 in

the CAM, a 0 in the address representing a 01 in the CAM, a don't care in the address

representing a 00 in the CAM, as disclosed in page 3.

28.   With respect to claim 82, RCP discloses a first group of address entries sharing a first

said address mask and a second group of address entries sharing a second said address mask, said

first and second groups being located at different locations of the CAM, as taught on page 3.

29.   With respect to claim 83, RCP discloses comprising at least one vacant

address entry location disposed within said CAM between said first and second groups of

address entries, as shown in figures 4, 5, and 7.

30.   With respect to claim 84, RCP discloses at least one vacant address entry location within

said CAM adjacent at least one of said address entry groups, as shown in figures 4, 5, and 7.

31.   With respect to claim 85, RCP discloses: receiving an address value in a comparand

register of said CAM; matching a further plurality of addresses, including a subset of said

communication system hierarchical addresses, to said address value; and outputting an output

hierarchical address of ,said further plurality of addresses according to respective storage locations of said further plurality of addresses, as shown in Table 7 on page 5.

32.   With respect to claim 86, RCP discloses wherein said output hierarchical address of said further plurality has a storage location lowest among said respective storage locations of said further plurality of addresses, as shown in Figure 2 on page 5.

33.   With respect to claim 87, RCP discloses wherein said further plurality of said communication system hierarchical addresses each includes at least one identical bit, as shown in Table 7 on page 5.

Conclusion

34.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-5931. The examiner can normally be reached on Monday-Friday, 2nd Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew D. Anderson
August 10, 2004